5. (Currently Amended): A system level device for battery and integrated circuit chip integration comprising:

at least one battery;

at least one integrated circuit chip powered by said at least one battery; and

a package connected to any of said at least one battery and said at least one integrated circuit chip,

wherein said at least one battery connects to a pair of opposed upright ends of said package, ~~and~~

wherein said at least one integrated circuit chip is disposed between said at least one battery and said package[[.]], and

wherein said at least one integrated circuit chip lays on top of a portion of said package.

6. (Original): The device of claim 3, wherein said at least one battery further comprises a stack of connected batteries.

7. (Currently Amended): A system level device for battery and integrated circuit chip integration comprising a multi-chip module integration system, wherein said multi-chip module integration system comprises:

a multi-chip module having a pair of opposed upright ends;

at least one battery connected to said multi-chip module; and

at least one integrated circuit chip connected to said battery, wherein said integrated circuit chip is powered by said battery, and wherein said at least one battery overhangs, and is larger than, said at least one integrated circuit chip[[.]],

wherein said at least one integrated circuit chip lays on top of a portion of said multi-chip module.

8. (Original): The device of claim 7, wherein said multi-chip module connects to said at least one integrated circuit chip through an interior portion of said multi-chip module.

9. (Previously Presented): The device of claim 7, wherein said at least one integrated circuit chip connects to an upper indent portion of said multi-chip module.

10. (Currently Amended): A system level device for battery and integrated circuit chip integration comprising a multi-chip module integration system, wherein said multi-chip module integration system comprises:

a multi-chip module;

at least one battery connected to said multi-chip module; and

at least one integrated circuit chip connected to said battery, wherein said integrated circuit chip is powered by said battery,

wherein said at least one battery connects to a pair of opposed upright ends of said multi-chip module, ~~and~~

wherein said at least one battery overhangs, and is larger than, said at least one integrated circuit chip[[.]], and

wherein said at least one integrated circuit chip lays on top of module.

11. (Currently Amended): An integrated chip structure comprising an integrated circuit chip;

a battery directly connected to said integrated circuit chip; and

a package having a pair of opposed upright ends, said package battery and said integrated circuit chip,

wherein said integrated circuit chip is disposed between said ba package[[.]], and

wherein said integrated circuit chip lays on top of a portion of s

12. (Original): The structure in claim 11, further comprising solde battery and said integrated circuit chip.

13. (Original): The structure in claim 12, wherein said solder conn electrical connection between said battery and said integrated circuit ch

14. (Previously Presented): The structure in claim 11, wherein said battery and said integrated circuit chip.

15. (Original): The structure in claim 12, wherein said battery is dir package.

5. (Currently Amended): A system level device for battery and integrated circuit chip integration comprising:

at least one battery;

at least one integrated circuit chip powered by said at least one battery; and

a package connected to any of said at least one battery and said at least one integrated circuit chip,

wherein said at least one battery connects to a pair of opposed upright ends of said package, ~~and~~

wherein said at least one integrated circuit chip is disposed between said at least one battery and said package[[.]], and

wherein said at least one integrated circuit chip lays on top of a portion of said package.

6. (Original): The device of claim 3, wherein said at least one battery further comprises a stack of connected batteries.

7. (Currently Amended): A system level device for battery and integrated circuit chip integration comprising a multi-chip module integration system, wherein said multi-chip module integration system comprises:

a multi-chip module having a pair of opposed upright ends;

at least one battery connected to said multi-chip module; and

at least one integrated circuit chip connected to said battery, wherein said integrated circuit chip is powered by said battery, and wherein said at least one battery overhangs, and is larger than, said at least one integrated circuit chip[[.]],

wherein said at least one integrated circuit chip lays on top of a portion of said multi-chip module.

8. (Original): The device of claim 7, wherein said multi-chip module connects to said at least one integrated circuit chip through an interior portion of said multi-chip module.

9. (Previously Presented): The device of claim 7, wherein said at least one integrated circuit chip connects to an upper indent portion of said multi-chip module.

10. (Currently Amended): A system level device for battery and integrated circuit chip integration comprising a multi-chip module integration system, wherein said multi-chip module integration system comprises:

a multi-chip module;

at least one battery connected to said multi-chip module; and

at least one integrated circuit chip connected to said battery, wherein said integrated circuit chip is powered by said battery,

wherein said at least one battery connects to a pair of opposed upright ends of said multi-chip module, ~~and~~

wherein said at least one battery overhangs, and is larger than, said at least one integrated circuit chip[[.]], and

wherein said at least one integrated circuit chip lays on top of a portion of said multi-chip module.

11. (Currently Amended): An integrated chip structure comprising:

an integrated circuit chip;

a battery directly connected to said integrated circuit chip; and

a package having a pair of opposed upright ends, said package connected to any of said battery and said integrated circuit chip,

wherein said integrated circuit chip is disposed between said battery and said package[[.]], and

wherein said integrated circuit chip lays on top of a portion of said package.

12. (Original): The structure in claim 11, further comprising solder connections between said battery and said integrated circuit chip.

13. (Original): The structure in claim 12, wherein said solder connections comprise an electrical connection between said battery and said integrated circuit chip.

14. (Previously Presented): The structure in claim 11, wherein said package surrounds said battery and said integrated circuit chip.

15. (Original): The structure in claim 12, wherein said battery is directly connected to said package.

16. (Currently Amended): An integrated chip structure comprising:

a package having a pair of opposed upright ends;

an integrated circuit chip mounted on said package;

a battery directly connected to said package and electrically connected to said integrated circuit chip,

wherein said integrated circuit chip is disposed between said battery and said package[[.]], and

wherein said integrated circuit chip lays on top of a portion of said package.

17. (Original): The structure in claim 16, wherein said battery is held adjacent to said integrated circuit chip by said package.

18. (Original): The structure in claim 16, wherein said package is between said battery and said integrated circuit chip.

19. (Previously Presented): The structure in claim 16, wherein said battery is electrically connected to said integrated circuit chip through said battery.

20. (Original): The structure in claim 16, wherein said battery comprises multiple batteries stacked on said package.